IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Tsai	Art Unit: 2182
Serial No.: 09/535,226	Confirmation No.: 2779
Filed: March 24, 2000	Examiner: Joshua D. Schneider
	Docket: TI-29058

For: INTERFACE BETWEEN DIFFERENT CLOCK RATE COMPONENTS

Appeal Brief under 37 C.F.R. §41.37

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §41.37 and the Notice of Appeal filed February 12, 2007.

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Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated, a corporation of Delaware with its principle place of business in Dallas, Texas. An assignment to Texas Instruments Incorporated is recorded at reel 013395 and frames 0377 and 0378.

Related Appeals and Interferences

There are no appeals of interferences related to this appeal in this application.

Status of the Claims

Claims 1 to 4 are rejected and subject to this appeal. No claims are allowed. Claims 5 to 14 are canceled.

Status of Amendments Filed After Final Rejection

No amendments to the claims were proposed following the FINAL REJECTION of October 11, 2006.

Summary of Claimed Subject Matter

The claimed subject matter is as follows:

Claim 1	Disclosure
A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate,	circuit illustrated in Figure 4 first component is low clock rate component 21, page 10, lines 9 and 10 second component is high clock rate component 22, page 10, line 10
a first buffer coupled to said first component, said first buffer receiving and storing data received from said first component at said first clock rate;	first buffer is ping buffer 23, page 10, lines 18 to 20
a second buffer coupled to said second component, said second buffer supplying data recalled therefrom to said second component at said second clock rate; and	second buffer is pong buffer 24, page 10, lines 20 and 21
a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.	copy/access controller is copy/access controller 24, page 10, line 21 to page 11, line 7 page 10, lines 21 to 23, page 11, lines 3 to 7 page 10, lines 23 to 26

Claim 2	Description
both said first buffer and said second buffer are random-access memories	page 4, lines 12 and 13 page 7, lines 21 to 23 page 11, lines 8 to 12

Claim 3	Description
both said first buffer and said second buffer are shift registers	page 4, lines 12 and 13 page 7, lines 21 to 23 page 11, lines 8 to 12

Claim 4	Description
said circuit is integrated onto a semiconductor die with one of said first component or said second component	page 4, lines 13 and 14 page 9, lines 21 to 24

Grounds for Rejection to be Reviewed on Appeal

Claims 1 to 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443 and Steinmetz et al U.S. Patent 5,809,521.

Arguments

Claims 1 recites subject matter not made obvious by the combination of Frankel et al and Steinmetz et al. Claim 1 recites a copy/access controller "operable to copy data from said first buffer to said second buffer when said first buffer is substantially full" and "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." These limitations are not made obvious by the combination of Frankel et al and Steinmetz et al. The FINAL REJECTION cites: input data register 10 of Frankel et al as making obvious the claimed first buffer; output data register 14 of Frankel et al as making obvious the recited second buffer; and the elements RAM 16, RAM address counters 16a, RAM input holding register 18, RAM output holding register 20 and write and read sequence generator and control logic of Frankel et al as making obvious the recite copy/access controller. Presumably the recited first component is the apparatus supplying data to input data register 10 and the recited second component is the apparatus receiving data form output data register 14. The FINAL REJECTION states at page 3, lines 8 to 11:

> "Frankel fails to explicitly teach the prompting of a second component to access the second buffer when the data is copied from the first buffer. However, it was notoriously well known in the art at the time of invention to use signal to prompt buffer connected devices to read and write data to and from the buffer."

The Applicant agrees with this statement of the Examiner. Frankel et at states at column 3, lines 59 to 63:

> "In a similar manner, the data is output from the buffer at the output data register 14 synchronously with the output data clock. When the output data register 14 is empty, data in the RAM output register 20 is transferred to it."

This portion of Frankel et al teaches continuous output of data from output data register 14 to the second component not shown. This portion of Frankel et al fails to teach prompting this second component "to access said second buffer when said data is copied from said first buffer" as recited in claim 1. Instead, this language strongly implies that access by the second component to data stored in the second buffer does not require any such prompting. The Applicant submits that the above quoted language of claim 1 requires more than merely writing to the output shift register. This language requires generation of a prompt signal by the copy/access controller to initiate reading data by the second component. The Applicant submits this limitation is not inherent in the mere writing of data to the buffer. The FINAL REJECTION cites element 16 and nEMPTY signal illustrated in Figure 1b and column 3, line 40 to column 4, line 5 of the secondary reference Steinmetz et al as making obvious this subject matter. Steinmetz et al states at column 3, line 62 to column 4, line 1 (within the section cited by the Examiner):

> "Each FIFO memory is cascaded by connecting the 'not empty' (nEMPTY) signal of one FIFO to the write terminal of the succeeding FIFO, the 'not full' (nFULL) signal to the read terminal of the preceding FIFO and the data output terminal (DATAOUT) of one FIFO to the data input (DATAIN) terminal of the succeeding FIFO."

The Applicant assumes that the Examiner's position is that the nEMPTY signal of FIFO 16 causes the not illustrated receiving system to access data for read out from FIFO 16. This teaching of Steinmetz et al differs from the above quoted language of claim 1 because there is not a single structure (the claimed copy/access controller) which both copies data to the second buffer and prompts the second component to access the second buffer. This subject

matter is illustrated at element 24 in Figure 4 of this application. Note that in Steinmetz et al writing to FIFO 16 is caused by the nEMPTY signal of FIFO 14 coupled to the WRITE input of FIFO 16. However, FIFO 14 does not prompt the second component to access this data in FIFO 16 are required by claim 1. Instead, the nEMPTY signal of FIFO 16 makes this prompt. In particular, there is no disclosure in Steinmetz et al that the nEMPTY signal of a FIFO is generated by the same component that copies data into the second buffer. The FINAL REJECTION states at page 2, lines 6 to 11:

> "Applicant also argues that Stienmetz is differentiated because of a lack of a single structure. This argument also does not address the rejection as stated. The teaching of a single structure is clearly shown in the primary reference, Frankel. If the teaching of a single structure was found in Steinmetz, there would have been no need for any of the teachings of Frankel, and Stienmetz could have been used in an anticipation rejection."

The Applicant respectfully submits that neither Frankel et al nor Steinmetz et al teach the recited copy/access controller. Particularly, neither Frankel et al nor Steinmetz et al teach the recited copy/access controller which both operates "to copy data from said first buffer to said second buffer when said first buffer is substantially full" and "to prompt said second component to access said second buffer when said data is copied from said first buffer." Accordingly, claim 1 is allowable over the combination of Frankel et al and Steinmetz et al.

The ADVISORY ACTION of January 30, 2007 in this application states:

> "Applicant argues that Frankel does not teach the signals of the claimed controller. This argument does not address the rejection as a whole. Applicant also argues that Steinmetz does not teach a single structure for generating control

> signals. Again, this argument does not address the rejection as a whole. Applicants arguments attack the references singularly without ever addressing the actual rejection which requires ans (sic) of the combined references. This is not an anticipation rejection, but rather a rejection which requires an analysis of what the art as a whole would have suggested to one of ordinary skill at the time of invention."

The Applicant's argument follows the contours of the FINAL REJECTION. The FINAL REJECTION states page 3, lines 8 to 11 (quoted above) that Frankel et al fails to "explicitly teach" the generation of a prompt signal by the copy/access controller to initiate reading data by the second component of claim 1. The FINAL REJECTION then cites portions of Steinmetz et al as allegedly teaching this limitation. The Applicant believes that the above arguments demonstrate that Steinmetz et al fails to make obvious this limitation. If the Applicant's arguments are correct, then the FINAL REJECTION fails to cite any portion of either reference as making obvious this limitation. Accordingly no amount of "rejection as a whole" and "obvious to one of ordinary skill in the art at the time of invention to combine" can support the rejection.

Claims 2 to 4 are allowable by dependence upon respective allowable base claim 1.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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CLAIMS APPENDIX

1. A circuit for interfacing between a first component operating at a first clock rate and a second component operating at a second clock rate wherein said second clock rate is higher than said first clock rate, said circuit comprising:

a first buffer coupled to said first component, said first buffer receiving and storing data received from said first component at said first clock rate;

a second buffer coupled to said second component, said second buffer supplying data recalled therefrom to said second component at said second clock rate;

a copy/access controller connected to said first buffer, said second buffer, and said second component and operable to copy data from said first buffer to said second buffer when said first buffer is substantially full, and further operable to prompt said second component to access said second buffer when said data is copied from said first buffer.

2. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are random-access memories.

3. The circuit as set forth in Claim 1, wherein both said first buffer and said second buffer are shift registers.

4. The circuit as set forth in Claim 1, wherein said circuit is integrated onto a semiconductor die with one of said first component or said second component.

Evidence Appendix

None

Related Proceedings Appendix

None